## REMARKS

Objections to Drawings

FIGS. 10a to 12c have been amended to include the legend BACKGROUND ART. Amended drawings are submitted herewith.

Rejection of Claims 1, 3, 5-7, 9 and 11 Under 35 U.S.C. §102(e) based on *Ishitsuka et al.* (U.S. Patent No. 6,242,323)

The rejection of claims 1-3 and 5-6 will first be addressed.

The invention of amended claim 1 includes a semiconductor device having a trench element separation region that includes a trench formed in a surface of a semiconductor substrate, and that isolates separate semiconductor elements. The trench element separation region also includes an oxide film formed on inner walls of the trench and a trench filling insulating material filling the trench and having edges above the inner walls of the trench. The edges of the trench filling insulating material are defined by side edges of a sacrificial layer formed by a pullback etching process including a neutral radical. The pullback etching process is performed before the trench is filled. Inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.[1]

The cited reference does not show a trench filling insulating material defined by side edges of a sacrificial layer formed by a pullback etching process including a neutral radical.

As noted in Applicant's specification, a pullback etching "pulls back" the edges of a sacrificial layer.[2] Thus, in a pullback etch process, the edges of a sacrificial layer (and hence the inner wall edges of a trench filling material) are situated further from the edges of an originally formed sacrificial layer.

The cited reference, *Ishitsuka et al.*, does not show such a structure. In *Ishitsuka et al.*, no pullback etch is performed. In fact, *Ishitsuka et al.* teaches away from claim 1, as the reference

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[1] See Lindemann Maschinenefabrick GmbH v. American Hoist & Derrick Col., 221 USPQ 481, 485 (Fed. Cir. 1984).

[2] See the Specification, Page 4, Line 23 to Page 5, Line 2.

adds to a mask nitride layer, rather than etching back such a layer, prior to filling a trench.[3]

It is believed the pullback etch limitations of claim 1 provide concrete limitations that clearly differentiate the claimed invention from that of *Ishitsuka et al.*, as such limitations lead to a different resulting structure than that of *Ishitsuka et al.*

Thus, because the cited reference does not show all limitations of claim 1, this ground of rejection is traversed.

The rejection of claims 7, 9 and 11 will now be addressed.

Amended claim 7 is directed to a semiconductor device with a trench element separation region including a trench formed in a surface of a semiconductor substrate. The trench element separation region isolating a first doped channel layer of a first insulated gate field effect transistor (IGFET) from a second doped channel layer of a second IGFET. An oxide film formed on inner walls of the trench. In addition, a trench filling insulating material fills the trench and has edges above the inner walls of the trench defined by side edges of a sacrificial layer formed by a pullback etching process including a neutral radical. The pullback etching process is performed before the trench is filled. Inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

To the extent that this ground for rejection relies on the reference *Ishitsuka et al.*, the comments set forth above for claim 1 are incorporated by reference herein. Namely, that the reference does not show a trench filling insulating material edge defined by side edges of a sacrificial layer formed by a pullback etching process that includes a neutral radical.

Rejection of Claims 7 and 10 Under 35 U.S.C. §102(e) based on *Bhakta et al.* (U.S. Patent No. 6,258,697)

As noted in the previous response to office action, the cited reference *Bhakta et al.* does not show all the limitations of claim 7. The reference *Bhakta et al.* fails to show a trench filling insulating material edge defined by side edges of a sacrificial layer, as recited in claim 7.

*Bhakta et al.* discloses a semiconductor device having a trench that is filled with a filling material. However, edges of a filling material are not defined by side edges of a sacrificial layer,

[3] See *Ishitsuka et al.*, FIG. 18, and Col. 24, Lines 21-29.

but rather an oxide liner layer.

Applicant will now note this difference in more detail. The rejection equates a polish stop layer 34 of *Bhakta et al.* with Applicant's sacrificial layer, and trench filling material 46 of *Bhakta et al.* with Applicant's trench filling insulating material.

However, the edges of the trench filling material 46 of *Bhakta et al.* are not defined by the side edges of the polish stop layer 34 of *Bhakta et al.* If reference is made to FIG. 3C of *Bhakta et al.*, it is clearly shown that the edges of the trench filling material 46 are defined by oxide film 42 (shown by dashed lines in FIG. 3C).

Applicant believes the above provides a clear showing that *Bhakta et al.* does not show all limitations of claim 7. For this reason, this ground of rejection is traversed.

Claims 1 and 7 have been amended. Such amendment further detail Applicant's etching process, and so should not necessitate a new search.

Further, Applicant requests that such amendments be entered for purposes of appeal.

The present claims 1, 3, 5-7, and 9-11 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Version With Markings to Show Changes Made

In the Claims.

1. (Amended) A semiconductor device, comprising:

a trench element separation region including a trench formed in a surface of a semiconductor substrate, the trench element separation region isolating separate semiconductor elements;

an oxide film formed on inner walls of the trench;

a trench filling insulating material filling the trench and having edges above the inner walls of the trench that are defined by side edges of a sacrificial layer formed by **[an] a pullback** etching process including a neutral radical **that is performed before filling the trench**; and

wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

7. (Amended) A semiconductor device, comprising:

a trench element separation region including a trench formed in a surface of a semiconductor substrate, the trench element separation region isolating a first doped channel layer of a first insulated gate field effect transistor (IGFET) from a second doped channel layer of a second IGFET;

an oxide film formed on inner walls of the trench;

a trench filling insulating material filling the trench and having edges above the inner walls of the trench defined by side edges of a sacrificial layer formed by **[an] a pullback** etching process including a neutral radical **performed before filling the trench**; and

wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.